etching the second interlayer insulating layer, the second etching stopper, and the first interlayer insulating layer sequentially using the first etching stopper as an etching stopping point to form a via hole aligned with the lower conductive layer;

cont A'

forming a protective layer to protect a portion of the first etching stopper exposed at the bottom of the via hole, the protective layer filling the via hole;

etching a portion of the second interlayer insulating layer adjacent to the via hole using the second etching stopper as an etching stopping point to form a trench connected to the via hole;

removing the protective layer;

removing the portion of the first etching stopper positioned at the bottom of the via hole; and

forming an upper conductive layer that fills the via hole and the trench and is electrically connected to the lower conductive layer.